LMX2471 3.6 GHz Delta-Sigma Fractional-N PLL with 1.7 GHz Integer-N PLL

Check for Samples: LMX2471

FEATURES

- **Low in-band phase noise and low fractional spurs**
- **12 bit or 22 bit selectable fractional modulus**
- **Up to 4th order programmable delta-sigma modulator**
- **Enhanced Anti-Cycle Slip Fastlock Circuitry**
  - **Fastlock**
  - **Cycle slip reduction**
  - **Integrated timeout counters**
- **Digital lock detect output**
- **Prescalers allow wide range of N values**
  - **RF PLL: 16/17/20/21**
  - **IF PLL: 8/9 or 16/17**
- **Crystal Reference Frequency up to 110 MHz**
- **On-chip crystal reference frequency doubler.**
- **Phase Comparison Frequency up to 50 MHz**
- **Hardware and software power-down control**
- **Ultra low consumption: I_{CC} = 5.6 mA (typical)**

APPLICATIONS

- **Cellular Phones and Base Stations**
- **Applications requiring fine frequency resolution**
- **Satellite and Cable TV Tuners**
- **WLAN Standards**

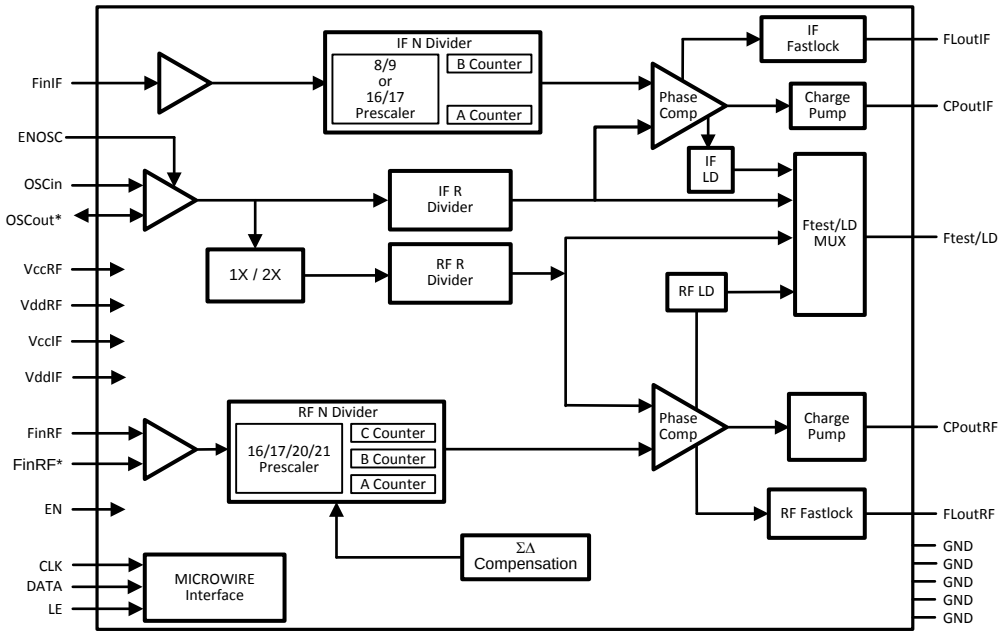
DESCRIPTION

The LMX2471 is a low power, high performance delta-sigma fractional-N PLL with an auxiliary integer-N PLL. The device is fabricated using National Semiconductor's advanced BiCMOS process.

With delta-sigma architecture, fractional spur compensation is achieved with noise shaping capability of the delta-sigma modulator and the inherent low pass filtering of the PLL loop filter. Fractional spurs at lower frequencies are pushed to higher frequencies outside the loop bandwidth. Unlike analog compensation, the digital feedback techniques used in the LMX2471 are highly resistant to changes in temperature and variations in wafer processing. With delta-sigma architecture, the ability to push close in spur and phase noise energy to higher frequencies is a direct function of the modulator order. The higher the order, the more this energy can be spread to higher frequencies. The LMX2471 has a programmable modulator up to order four, which allows the designer to select the optimum modulator order to fit the phase noise, spur, and lock time requirements of the system.

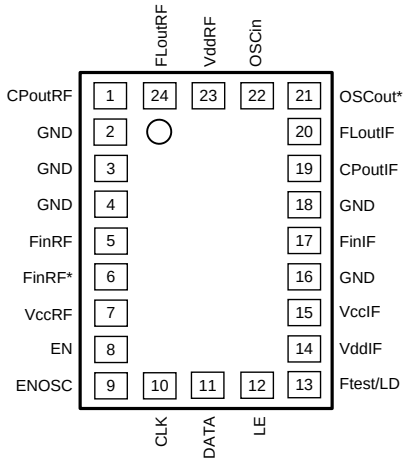
Programming is fast and simple. Serial data is transferred into the LMX2471 via a three line MICROWIRE interface (Data, Clock, Load Enable). Nominal supply voltage is 2.5 V. The LMX2471 features a typical current consumption of 5.6 mA at 2.5 V. The LMX2471 is available in a 24 lead 3.5 X 4.5 X 0.6 mm package.

Functional Block Diagram



Connection Diagram

Figure 1. 24-Pin CSP (SLE) Package



Pin Functions

Pin Descriptions

Pin #	Pin Name	I/O	Pin Description
1	CPoutRF	O	RF charge pump output.
2	GND	-	Ground
3	GND	-	RF Ground
4	GND	-	Ground for RF PLL digital circuitry.
5	FinRF	I	RF prescaler input. Small signal input from the VCO.
6	FinRF*	I	RF prescaler complimentary input. For single-ended operation, a bypass capacitor should be placed as close as possible to this pin and be connected directly to the ground plane.

Pin Descriptions (continued)

Pin #	Pin Name	I/O	Pin Description
7	VccRF		RF PLL power supply voltage input. Must be equal to VccIF . May range from 2.35V to 2.75V. Bypass capacitors should be placed as close as possible to this pin and be connected directly to the ground plane.
8	EN	I	Chip enable input. High impedance CMOS input. When EN is high, the chip is powered up, otherwise it is powered down.
9	ENOSC	I	This pin should be grounded for normal operation.
10	CLK	I	MICROWIRE Clock. High impedance CMOS Clock input. Data for the various counters is clocked into the 24 bit shift register on the rising edge.
11	DATA	I	MICROWIRE Data. High impedance binary serial data input.
12	LE		MICROWIRE Load Enable. High impedance CMOS input. Data stored in the shift registers is loaded into the internal latches when LE goes HIGH
13	Ftest/LD	O	Test frequency output / Lock Detect
14	VddIF	-	Digital power supply for IF PLL
15	VccIF	-	IF power supply voltage input. Must be equal to VccRF. Input may range from 2.35 V to 2.75 V. Bypass capacitors should be placed as close as possible to this pin and be connected directly to the ground plane.
16	GND	-	Ground for RF PLL digital circuitry.
17	FinIF	I	IF prescaler input. Small signal input from the VCO.
18	GND	-	Digital ground for IF PLL
19	CPoutIF	O	IF PLL charge pump output
20	FLoutIF	O	IF Fastlock Output. Also functions as Programmable TRI-STATE CMOS output.
21	OSCout*	I/O	Complementary reference input or oscillator output.
22	OSCin	I	Reference input
23	VddRF	-	Digital power supply for RF PLL
24	FLoutRF	O	RF Fastlock Output. Also functions as Programmable TRI-STATE CMOS output.

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Absolute Maximum Ratings (1) (2)

Parameter	Symbol	Value			Units
		Min	Typ	Max	
Power Supply Voltage	V_{CC}	-0.3		3.0	V
	V_{DD}	V_{CC}		V_{CC}	V
Voltage on any pin with GND =V_{SS} = 0V	V_i	-0.3		V_{CC} + 0.3	V
Storage Temperature Range	T_s	-65		+150	°C
Lead Temperature (Solder 4 sec.)	T_L			+260	°C

(1) “Absolute Maximum Ratings” indicate limits beyond which damage to the device may occur. "Recommended Operating Conditions" indicate conditions for which the device is intended to be functional, but do not guarantee specific performance limits. For guaranteed specifications and test conditions, see the Electrical Characteristics. The guaranteed specifications apply only for the test conditions listed. Note also that these maximum ratings imply that the voltage at all the power supply pins of VccRF, VccIF, VddRF, and VddIF are the same. V_{CC}will be used to refer to the voltage at these pins.

(2) This Device is a high performance RF integrated circuit with an ESD rating < 2 kV and is ESD sensitive. Handling and assembly of this device should only be done at ESD-free workstations.

Recommended Operating Conditions

Parameter	Symbol	Value			Units
		Min	Typ	Max	
Power Supply Voltage (1)	V_{CC}	2.25		2.75	V
	V_{DD}	V_{CC}		V_{CC}	V
Operating Temperature	T_A	-40		+85	°C

(1) “Absolute Maximum Ratings” indicate limits beyond which damage to the device may occur. "Recommended Operating Conditions" indicate conditions for which the device is intended to be functional, but do not guarantee specific performance limits. For guaranteed specifications and test conditions, see the Electrical Characteristics. The guaranteed specifications apply only for the test conditions listed. Note also that these maximum ratings imply that the voltage at all the power supply pins of VccRF, VccIF, VddRF, and VddIF are the same. V_{CC}will be used to refer to the voltage at these pins.

Electrical Characteristics

(V_{CC} = 2.5V; -40°C ≤ T_A ≤ +85°C unless otherwise specified)

Symbol	Parameter	Conditions	Value			Units
			Min	Typ	Max	
Icc PARAMETERS						
I_{CC}RF	Power Supply Current, RF Synthesizer	IF PLL OFF RF PLL ON Charge Pump TRI-STATE OSC=0		3.6	5.7	mA
I_{CC}IF	Power Supply Current, IF Synthesizer	IF PLL ON RF PLL OFF Charge Pump TRI-STATE OSC=0		2.0	2.7	mA
I_{CC}TOTAL	Power Supply Current, Entire Synthesizer	IF PLL ON RF PLL ON Charge Pump TRI-STATE OSC=0		5.6	8.5	mA
I_{CC}PD	Power Down Current	EN = ENOSC = 0V CLK, DATA, LE = 0V		1	15	µA
RF SYNTHESIZER PARAMETERS						
f_{FinRF}	Operating Frequency		500		3600	MHz
p_{FinRF}	Input Sensitivity		-15		0	dBm
f_{COMP}	Phase Detector Frequency				50	MHz
$I_{CPoutRF}$SRCE	RF Charge Pump Source Current	RF_CPG = 0 $V_{CPoutRF}$=V_{CC} /2		100		µA
		RF_CPG = 1 $V_{CPoutRF}$=V_{CC}/2		200		µA
		...		...		µA
		RF_CPG = 15 $V_{CPoutRF}$=V_{CC}/2		1600		µA
$I_{CPoutRF}$SINK	RF Charge Pump Sink Current	RF_CPG = 0 $V_{CPoutRF}$=V_{CC}/2		-100		µA
		RF_CPG = 1 $V_{CPoutRF}$=V_{CC}/2		-200		µA
		...		...		µA
		RF_CPG = 15 $V_{CPoutRF}$=V_{CC}/2		-1600		µA
$I_{CPoutRF}$TRI	RF Charge Pump TRI-STATE Current Magnitude	0.4 ≤ $V_{CPoutRF}$ ≤ V_{CC} -0.4		2	10	nA
$I_{CPoutRF}$%MIS	RF CP Sink vs. CP Source Mismatch	$V_{CPoutRF}$ = V_{CC}/2 T_A = 25°C		3	10	%
$I_{CPoutRF}$%V	RF CP Current vs. CP Voltage	0.4 ≤ $V_{CPoutRF}$ ≤ V_{CC} -0.4 T_A = 25°C		5	15	%
$I_{CPoutRF}$%TEMP	RF CP Current vs. Temperature	$V_{CPoutRF}$ = V_{CC}/2		8		%
IF SYNTHESIZER PARAMETERS						
f_{FinIF}	Operating Frequency		250		1700	MHz
p_{FinIF}	IF Input Sensitivity		-15		0	dBm
f_{COMP}	Phase Detector Frequency				10	MHz
$I_{CPoutIF}$SRCE	IF Charge Pump Source Current	IF_CPG = 0 $V_{CPoutIF}$ = V_{CC} /2		1		mA
		IF_CPG = 1 $V_{CPoutIF}$ = V_{CC}/2		4		mA
$I_{CPoutIF}$SINK	IF Charge Pump Sink Current	IF_CPG = 0 $V_{CPoutIF}$ = V_{CC}/2		-1		mA
		IF_CPG = 1 $V_{CPoutIF}$ = V_{CC}/2		-4		mA

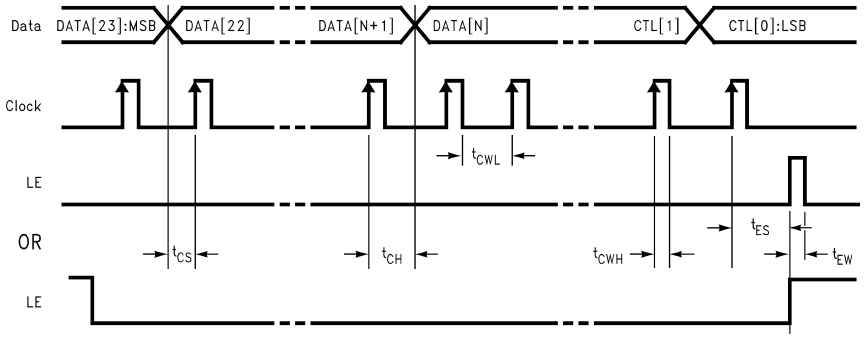
Electrical Characteristics (continued)

(V_{CC} = 2.5V; -40°C ≤ T_A ≤ +85°C unless otherwise specified)

Symbol	Parameter	Conditions	Value			Units
			Min	Typ	Max	
$I_{CPoutIF}$TRI	IF Charge Pump TRI-STATE Current Magnitude	0.4 ≤ $V_{CPoutIF}$ ≤ V_{CC} RF -0.4		2	10	nA
$I_{CPoutIF}$%MIS	IF CP Sink vs. CP Source Mismatch	$V_{CPoutIF}$ = V_{CC}/2 T_A = 25°C		3		%
$I_{CPoutIF}$%V	IF CP Current vs. CP Voltage	0.4 ≤ $V_{CPoutIF}$ ≤ V_{CC} -0.4 T_A = 25°C		8	15	%
$I_{CPoutIF}$%TEMP	IF CP Current vs. Temperature	$V_{CPoutIF}$ = V_{CC}/2		8		%
OSCILLATOR PARAMETERS						
f_{OSCin}	Oscillator Operating Frequency	OSC2X = 0	5		110	MHz
		OSC2X = 1	5		20	MHz
v_{OSCin}	Oscillator Input Sensitivity		0.5		V_{CC}	V
I_{OSCin}	Oscillator Input Current	OSC=0	-100		100	µA
DIGITAL INTERFACE (DATA, CLK, LE, EN, ENRF, Ftest/LD, FLoutRF, FLoutIF)						
V_{IH}	High-Level Input Voltage		1.6		V_{CC}	V
V_{IL}	Low-Level Input Voltage				0.4	V
I_{IH}	High-Level Input Current	V_{IH} = V_{CC}	-1.0		1.0	µA
I_{IL}	Low-Level Input Current	V_{IL} = 0 V	-1.0		1.0	µA
V_{OH}	High-Level Output Voltage	I_{OH} = -500 µA	V_{CC}-0.4			V
V_{OL}	Low-Level Output Voltage	I_{OL} = 500 µA			0.4	V
MICROWIRE INTERFACE TIMING						
T_{CS}	Data to Clock Set Up Time	See Microwire Input Timing	50			ns
T_{CH}	Data to Clock Hold Time	See Microwire Input Timing	10			ns
T_{CWH}	Clock Pulse Width High	See Microwire Input Timing	50			ns
T_{CWL}	Clock Pulse Width Low	See Microwire Input Timing	50			ns
T_{ES}	Clock to Load Enable Set Up Time	See Microwire Input Timing	50			ns
T_{EW}	Load Enable Pulse Width	See Microwire Input Timing	50			ns
PHASE NOISE						
L_{F1Hz}RF	RF Synthesizer Normalized Phase Noise Contribution (1)	RF_CPG = 0		-200		dBc/Hz
		RF_CPG = 3		-206		dBc/Hz
		RF_CPG = 7		-208		dBc/Hz
		RF_CPG = 15		-210		dBc/Hz
L_{F1Hz}IF	IF Synthesizer Normalized Phase Noise Contribution (1)	Applies to both low and high current modes OSC=0		-214		dBc/Hz

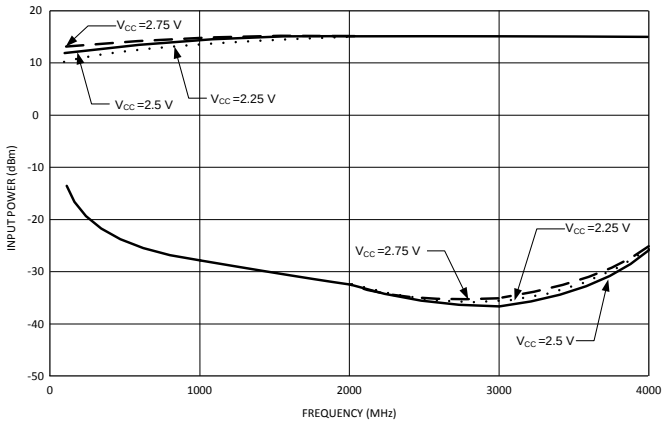
(1) Normalized Phase Noise Contribution is defined as: $L_N(f) = L(f) – 20\log(N) – 10\log(f_{COMP})$ where L(f) is defined as the single side band phase noise measured at an offset frequency, f, in a 1 Hz Bandwidth. The offset frequency, f, must be chosen sufficiently smaller than the PLL loop bandwidth, yet large enough to avoid substantial phase noise contribution from the reference source. The offset chosen was 4 KHz.

Figure 2. MICROWIRE INPUT TIMING DIAGRAM

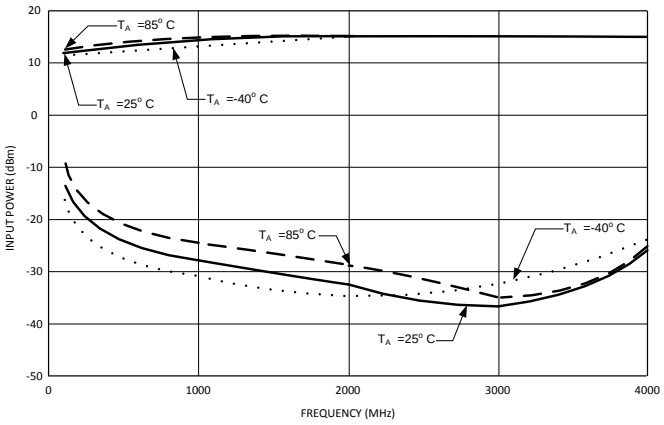


: Sensitivity

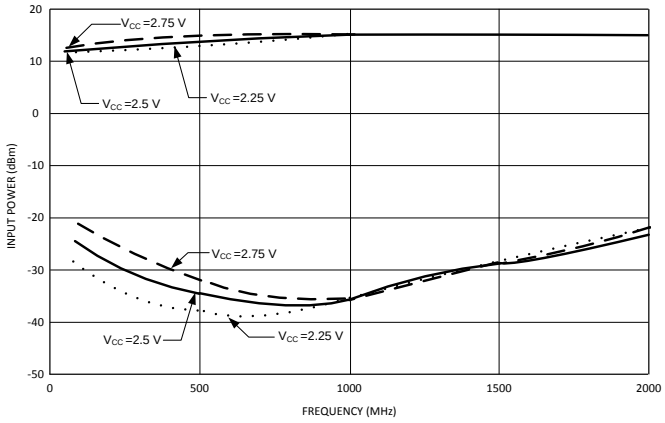
RF N Counter Sensitivity
T_A = 25°C



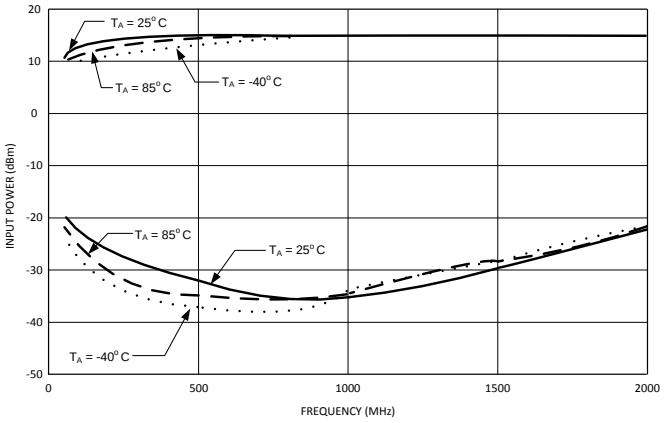
RF N Counter Sensitivity
V_{CC} = 2.5 V



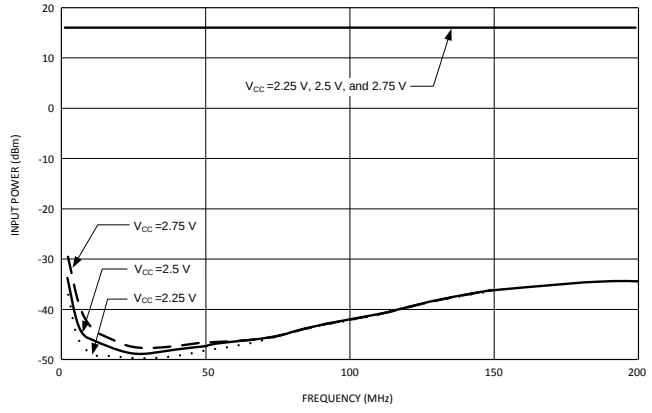
IF N Counter Sensitivity
T_A = 25°C



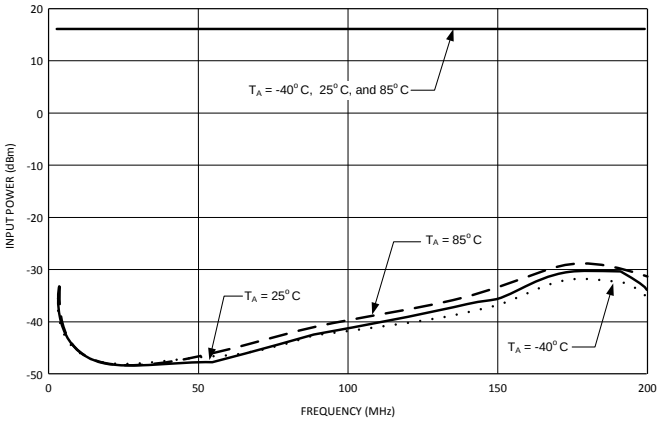
IF N Counter Sensitivity
V_{CC} = 2.5 V



OSCin Counter Sensitivity
OSC=0
T_A = 25° C

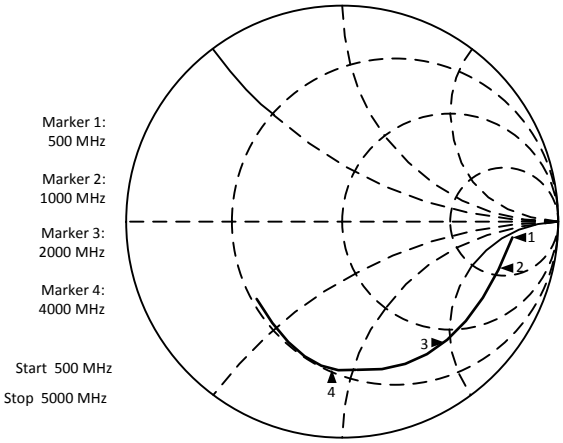


OSCin Counter Sensitivity
OSC=0
V_{CC}= 2.5 V



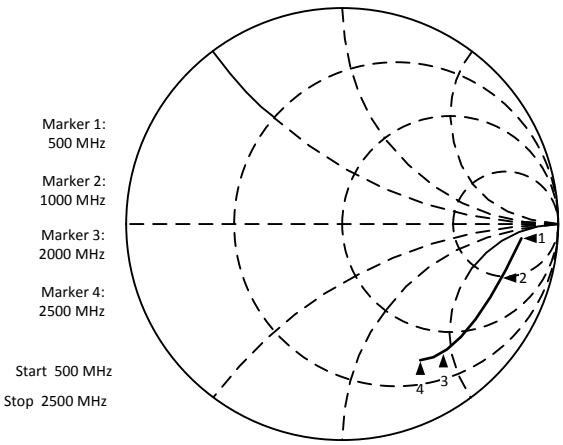
: Sensitivity (continued)

: FinRF Input Impedance



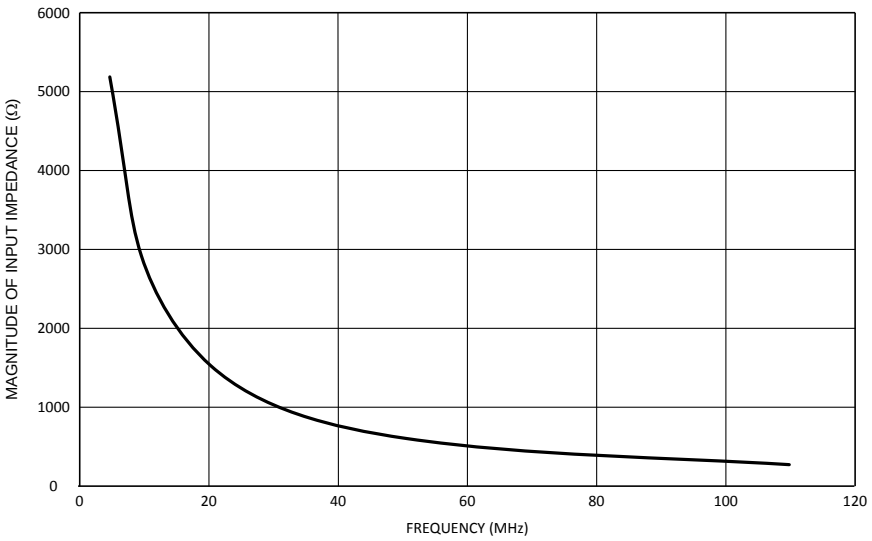
FinRF Input Impedance (V_{CC}=2.5 V, T_A=25° C)		
Frequency (MHz)	**Real (Ohms)**	**Imaginary (Ohms)**
500	389.9	-158.3
750	270.8	-186.8
1000	160.4	-172.3
1250	95.7	-144.7
1500	61.1	-120.0
1750	44.0	-104.5
2000	36.2	-95.6
2250	32.6	-90.4
2500	32.0	-86.3
2750	30.7	-80.5
3000	28.3	-74.6
3250	26.3	-65.2
3500	22.6	-57.4
3750	18.7	-49.9
4000	16.7	-44.1

: FinIF Input Impedance



FinIF Input Impedance (V_{CC}=2.5 V, T_A=25°C)		
Freqeuncy (MHz)	**Real (Ohms)**	**Imaginary (Ohms)**
500	377.4	-174.6
600	325.4	-186.6
700	272.7	-192.6
800	222.6	-191.1
900	178.2	-182.4
1000	143.0	-170.6
1100	113.8	-157.1
1200	92.6	-144.5
1300	76.5	-133.0
1400	64.1	-123.0
1500	55.2	-114.9
1600	48.5	-108.2
1700	43.3	-102.9
1800	39.4	-98.4
1900	36.4	-94.6
2000	34.5	-91.6

: OSCin Input Impedance



OSCin Input Impedance (V_{CC}=2.5 V, T_A=25 °C)			
Frequency (MHz)	**Real (Ohms)**	**Imaginary (Ohms)**	**Magnitude (Ohms)**
50	2200	-4700	5189
10	710	-2700	2792
20	229	-1500	1517
30	133	-988	997
40	93	-752	758
50	74	-606	611
60	62	-505	509
70	53	-435	438

OSCin Input Impedance (V_{CC}=2.5 V, T_A=25 °C)			
Frequency (MHz)	**Real (Ohms)**	**Imaginary (Ohms)**	**Magnitude (Ohms)**
80	49	-382	385
90	45	-341	344
100	42	-309	312
110	40	-282	285

: Currents

Figure 3. Total Current Consumption
OSC=0

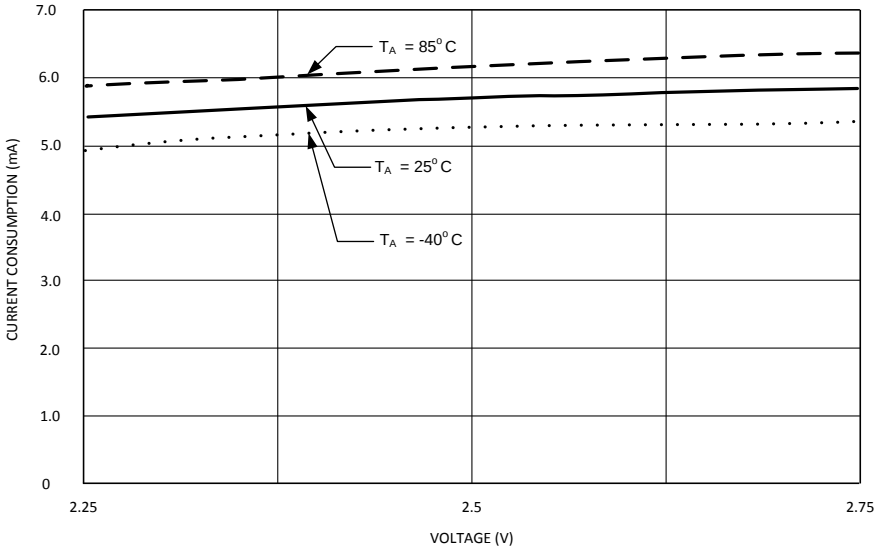


Figure 4. Powerdown Current
EN = LOW

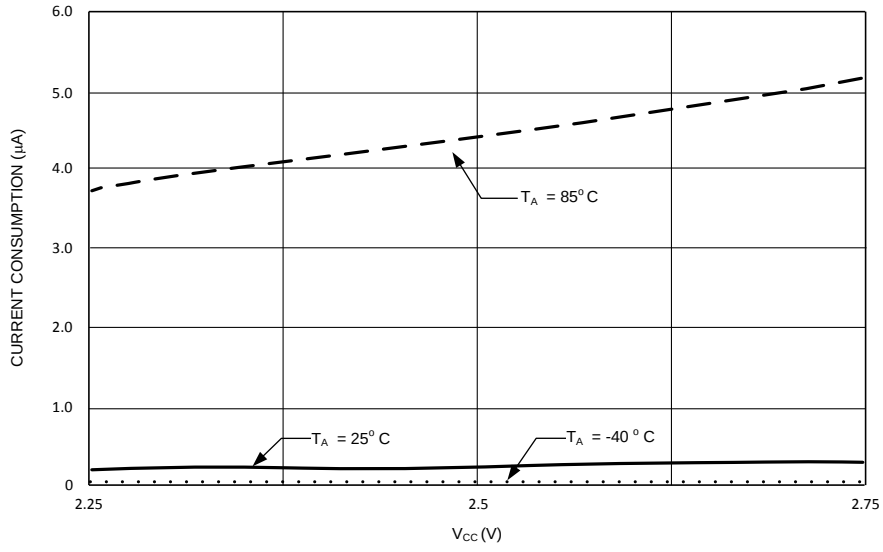


Figure 5. RF Charge Pump Current
V_{CC} = 2.5 Volts

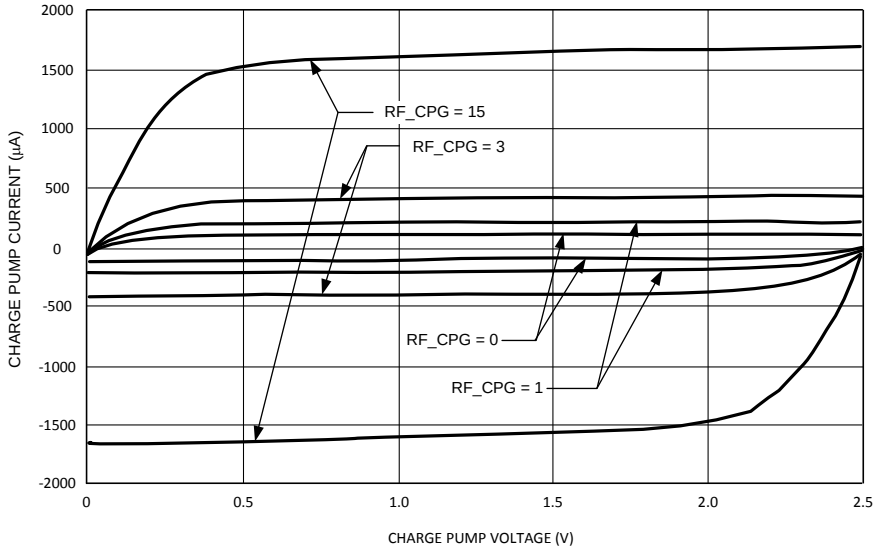


Figure 6. IF Charge Pump Current
V_{CC} = 2.5 Volts

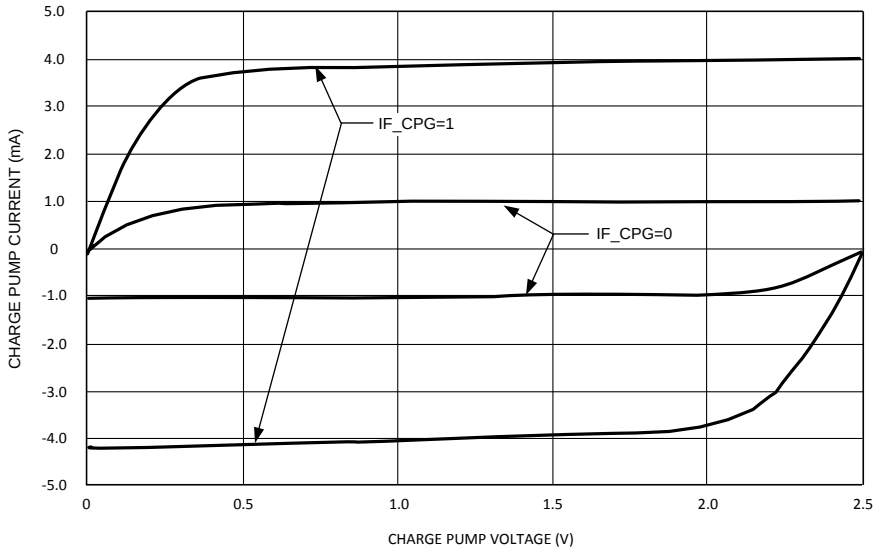


Figure 7. Charge Pump Leakage
RF PLL

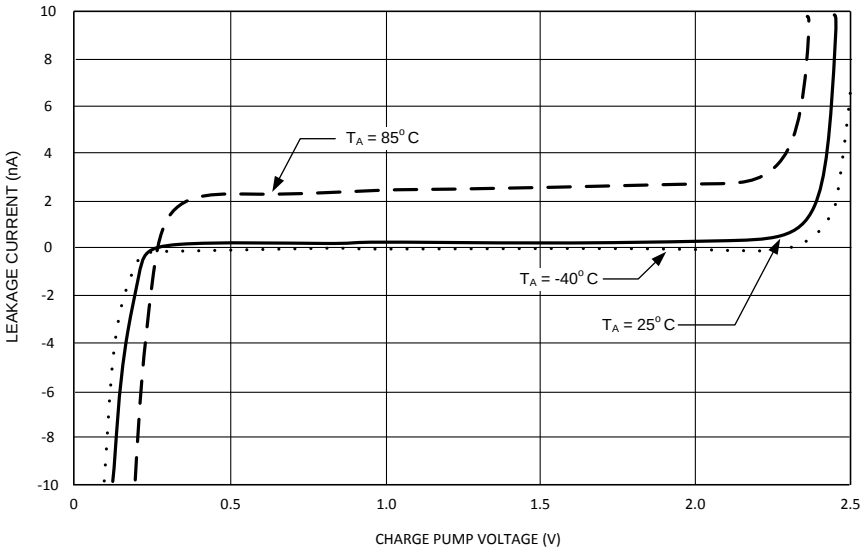
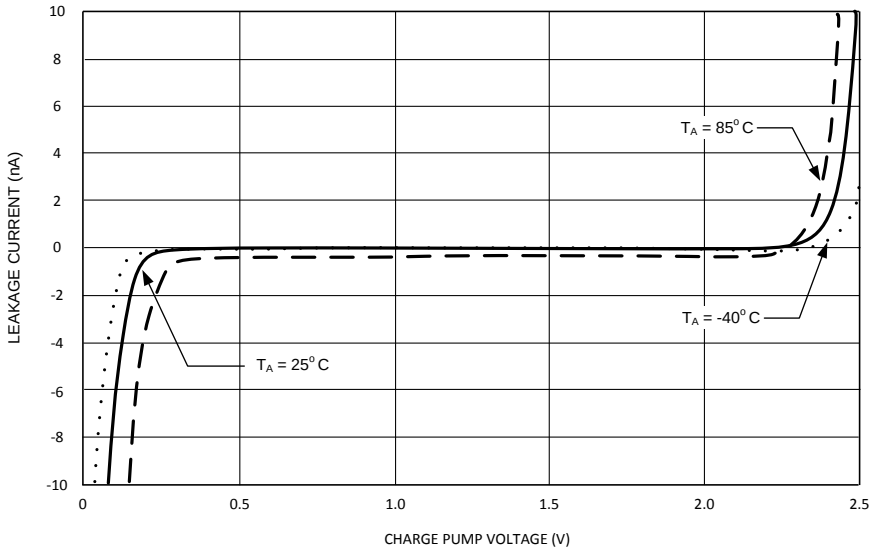


Figure 8. Charge Pump Leakage
IF PLL

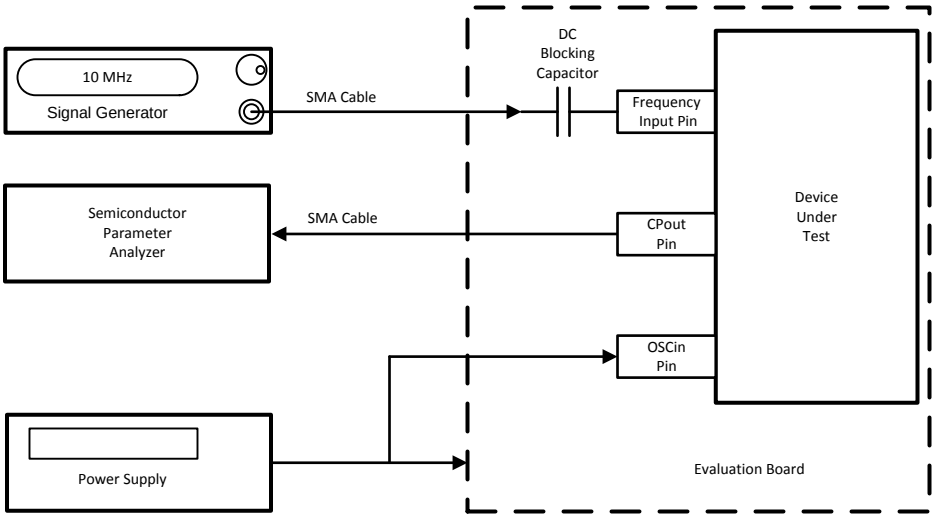


The input impedance of the FinRF, FinIF, and OSCin pins does not change significantly with voltage or temperature. The impedance of the FinRF and FinIF pins also does not change much when the PLL is powered up or down.

Typical performance characteristics do not imply any sort of guarantee. Guaranteed specifications are in the electrical characteristics section.

Bench Test Setups

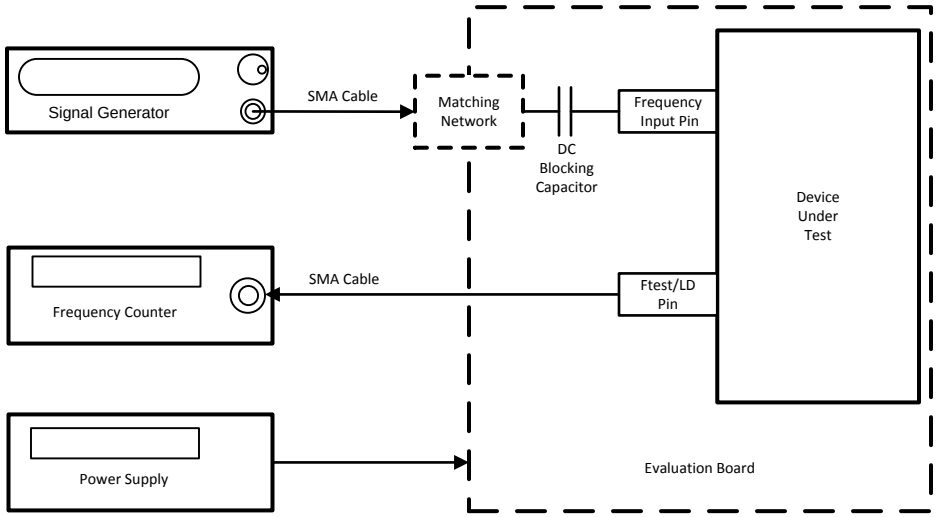
CHARGE PUMP CURRENT MEASUREMENT PROCEDURE



The above block diagram shows the test procedure for testing the RF and IF charge pumps. These tests include absolute current level, mismatch, and leakage. In order to measure the charge pump currents, a signal is applied to the high frequency input pins. The reason for this is to guarantee that the phase detector gets enough transitions in order to be able to change states. If no signal is applied, it is possible that the charge pump current reading will be low due to the fact that the duty cycle is not 100%. The OSCin Pin is tied to the supply. The charge pump currents can be measured by simply programming the phase detector to the necessary polarity. For instance, in order to measure the RF charge pump current, a 10 MHz signal is applied to the FinRF pin. The source current can be measured by setting the RF PLL phase detector to a positive polarity, and the sink current can be measured by setting the phase detector to a negative polarity. The IF PLL currents can be measured in a similar way. Note that the magnitude of the RF and IF PLL charge pump currents are also controlled by the RF_CPG and IF_CPG bits. Once the charge pump currents are known, the mismatch can be calculated as well. In order to measure leakage currents, the charge pump current is set to a TRI-STATE mode by enabling the counter reset bits. This is RF_RST for the RF PLL and IF_RST for the IF PLL. The table below shows a summary of the various charge pump tests.

Current Test	RF_CPG	RF_CPP	RF_CPT	IF_CPG	IF_CPP	IF_CPT
RF Source	0 to 15	0	0	X	X	X
RF Sink	0 to 15	1	0	X	X	X
RF TRI-STATE	X	X	1	X	X	X
IF Source	X	X	X	0 to 1	0	0
IF Sink	X	X	X	0 to 1	1	0
IF TRI-STATE	X	X	X	X	X	1

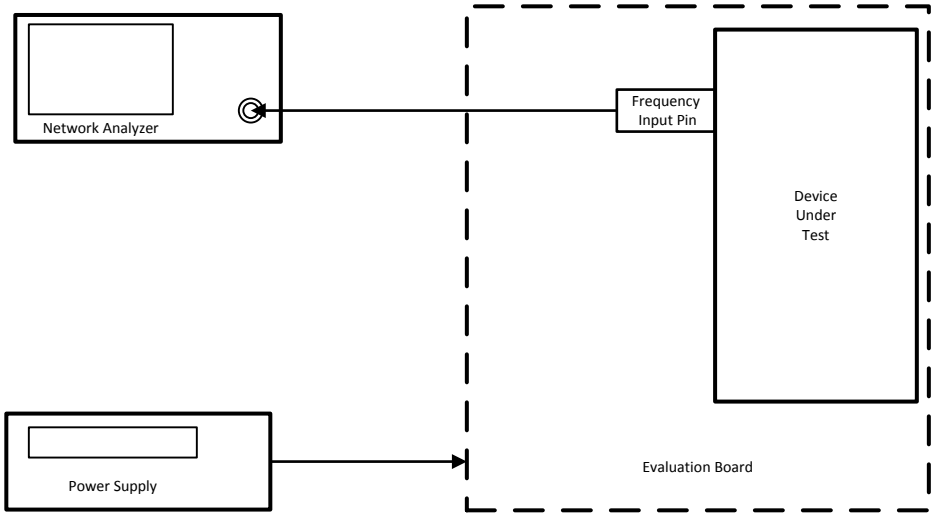
SENSITIVITY MEASUREMENT PROCEDURE



Frequency Input Pin	DC Blocking Capacitor	Corresponding Counter	Default Counter Value	MUX Value	OSC
OSCin	1000 pF	RF_R / 2	50	14	0
FinRF	47 pF	RF_N / 2	500	15	X
FinIF	100 pF	IF_N / 2	500	13	X

Sensitivity is defined as the power level limits beyond which the output of the counter being tested is off by 1 Hz or more of its expected value. It is typically measured over frequency, voltage, and temperature. In order to test sensitivity, the MUX[3:0] word is programmed to the appropriate value. The counter value is then programmed to a fixed value and a frequency counter is set to monitor the frequency of this pin. The expected frequency at the Ftest/LD pin should be the signal generator frequency divided by twice the corresponding counter value. The factor of two comes in because the LMX2471 has a flip-flop which divides this frequency by two to make the duty cycle 50% in order to make it easier to read with the frequency counter. The frequency counter input impedance should be set to high impedance. In order to perform the measurement, the temperature, frequency, and voltage is set to a fixed value and the power level of the signal is varied. The power level at the part is assumed to be 4 dB less than the signal generator power level. This accounts for 1 dB for cable losses and 3 dB for the pad. The power level range where the frequency is correct at the Ftest/LD pin to within 1 Hz accuracy is recorded for the sensitivity limits. The temperature, frequency, and voltage can be varied in order to produce a family of sensitivity curves. Since this is an open-loop test, the charge pump is set to TRI-STATE and the unused side of the PLL (RF or IF) is powered down when not being tested. For this part, there are actually four frequency input pins, although there is only one frequency test pin (Ftest/LD). The conditions specific to each pin are show above. The LMX2471 has a test bit that may be useful in debugging sensitivity problems at the FinRF pin. The location of this bit is R6[22] and should always be set to 0 for normal operation. If this bit is set to 1, then the sensitivity is degraded. When one suspects a sensitivity problem, try setting this bit to 1 and see what happens. If the problem is unaffected, it is likely not to be a sensitivity problem at the FinRF pin.

INPUT IMPEDANCE MEASUREMENT PROCEDURE



The above block diagram shows the test procedure measuring the input impedance for the LMX2471. This applies to the FinRF, FinIF, and OSCin pins and is measured in a 50 ohm environment. The basic test procedure is to calibrate the network analyzer, ensure that the part is powered up, and then measure the input impedance. The network analyzer can be calibrated by using either calibration standards or by soldering resistors directly to the evaluation board. An open can be implemented by putting no resistor, a short can be implemented by using a 0 ohm resistor, and a load can be implemented by using two 100 ohm resistors in parallel. Note that no DC blocking capacitor is used for this test procedure. This is done with the PLL removed from the PCB. This requires the use of a clamp down fixture that may not always be generally available. If no clamp down fixture is available, then this procedure can be done by calibrating up to the point where the DC blocking capacitor usually is, and then adding a 0 ohm resistor back for the actual measurement. Once that the network analyzer is calibrated, it is necessary to ensure that the PLL is powered up. This can be done by toggling the power down bits (RF_PD and IF_PD) and observing that the current consumption indeed increases when the bit is disabled. Sometimes it may be necessary to apply a signal to the OSCin pin in order to program the part. If this is necessary, disconnect the signal once it is established that the part is powered up. It is useful to know the input impedance of the PLL for the purposes of debugging RF problems and designing matching networks. Another use of knowing this parameter is make the trace width on the PCB such that the input impedance of this trace matches the real part of the input impedance of the PLL frequency of operation. In general, it is good practice to keep trace lengths short and make designs that are relatively resistant to variations in the input impedance of the PLL.

Functional Description

GENERAL

The basic phase-lock-loop (PLL) configuration consists of a high-stability crystal reference oscillator, a frequency synthesizer such as the National Semiconductor LMX2471, a voltage controlled oscillator (VCO), and a passive loop filter. The frequency synthesizer includes a phase detector, current mode charge pump, as well as programmable reference [R] and feedback [N] frequency dividers. The VCO frequency is established by dividing the crystal reference signal down via the R counter to obtain a frequency that sets the comparison frequency. This comparison frequency, f_{COMP}, is input of a phase/frequency detector and compared with another signal, f_N, the feedback signal, which was obtained by dividing the VCO frequency down by way of the N counter and fractional circuitry. The phase/frequency detector's current source outputs a charge into the loop filter, which is then converted into the VCO's control voltage. The function of the phase/frequency comparator is to adjust the voltage presented to the VCO until the frequency and phase of the feedback signal match that of the reference signal. When this ‘phase-locked’ condition exists, the VCO frequency will be N+F times that of the comparison frequency, where N is the integer component of the divide ratio and F is the fractional component. Fractional synthesis allows the phase detector frequency to be increased while maintaining the same frequency step size for channel selection. The division value N is thereby reduced giving a lower phase noise referred to the phase detector input, and the comparison frequency is increased allowing faster switching times.

PHASE DETECTOR OPERATING FREQUENCY

The maximum phase detector operating frequency for the LMX2471 is 50 MHz. However, this is not possible in all circumstances due to illegal divide ratios of the N counter. The crystal reference frequency also limits the phase detector frequency. There are trade-offs in choosing what phase detector frequency to operate at. If this frequency is run higher, then phase noise will be lower, but lock time may be increased due to cycle slipping. After this phase detector frequency gets sufficiently high, then there are diminishing returns for phase noise, and raising the charge pump current has a greater impact on phase noise. This phase detector frequency also has an impact on fractional spurs. In general, the spur performance is better at higher phase detector frequencies, although this is application specific. The current consumption may also slightly increase with higher phase detector frequencies.

OSCILLATOR

The LMX2471 provides maximum flexibility for choosing an oscillator reference. One possible method is to use a single-ended TCXO to drive the OSCin pin. The part can also be configured to be driven differentially using the OSCin and OSCout* pins. Note that the OSCin and OSCout* pins can not be used as an inverter for a crystal. Selection between these two modes does have a noticeable impact on phase noise and sub-fractional spurs. Regardless of which mode is used, the performance is generally best for higher oscillator power levels.

POWER DOWN AND POWER UP MODES

The power down state of the LMX2471 is controlled by many factors. The one factor that overrides all other factors is the EN pin. If this pin is low, this guarantees the part will be powered down. Asserting a high logic level on EN is necessary to power up the chip, however, there are other bits in the programming registers that can override this and put the PLL back in a power down state. Provided that the voltage on the EN pin is high, programming the RF_PD and IF_PD bits to zero guarantees that the part will be powered up. Programming either one of these bits to one will power down the appropriate section of the synthesizer, provided that the ATPU[1:0] (Auto Power Up) bits do not override this.

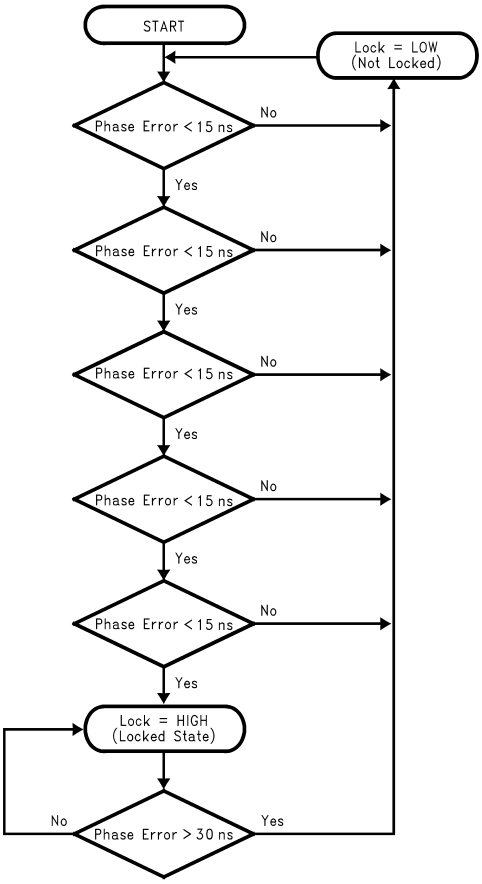
There are many different ways to power down this chip and many different things that can be powered down. This section discusses how to power down the PLLs on the chip. There are two terms that need to be defined first: synchronous power down and asynchronous power down. In the case of synchronous power down, the PLL chip powers down after the charge pump turns off. This is best to prevent unwanted frequency glitches upon power up. However, in certain cases where the charge pump is stuck on, such as the case when there is no VCO signal applied, this type of power down will not reliably work and asynchronous power down is necessary. In the case of asynchronous power down, the PLL powers down regardless of the status of the charge pump. There are 4 factors that affect the power down state of the chip: the EN pin, the power down bit, the TRI-STATE bit, and writing to the RF N counter with the RF_ATPU[1:0] bits enabled

EN Pin	ATPU[1:0] Bits Enabled + RF N Counter Written To	RF_PD Bit	RF_CPT Bit	PLL State
Low	X	X	X	Asynchronous Power Down
High	Yes	X	X	PLL is active with charge pump in the active state.
High	No	0	0	PLL is active with charge pump in the active state.
High	No	0	1	PLL is active, but charge pump is TRI-STATE.
High	No	1	0	Synchronous Power Down
High	No	1	1	Asynchronous Power Down

DIGITAL LOCK DETECT OPERATION

The RF PLL digital lock detect circuitry compares the difference between the phase of the inputs of the phase detector to a RC generated delay of 10 nS. To enter the locked state (Lock = HIGH) the phase error must be less than the 10nS RC delay for 5 consecutive reference cycles. Once in lock (Lock = HIGH), the RC delay is changed to approximately 20nS. To exit the locked state (Lock = LOW), the phase error must become greater than the 20nS RC delay. When the PLL is in the power down mode, Lock is forced LOW. For the RF PLL, the digital lock detect circuitry does not function reliably for comparison frequencies above 20 MHz.

The IF PLL digital lock detect circuitry works in a very similar way as the RF PLL digitial lock circuitry, except that it uses a delay of less than 15 nS for 5 reference cycles to determine a locked condition and a delay of greater than 30 nS to determine the IF PLL is unlocked. Note that if the MUX[3:0] word is set such as to view lock detect for both PLLs, an unlocked (LOW) condition is shown whenever either one of the PLLs is determined to be out of lock. A flow chart of the IF digital lock detect circuitry is shown below.



PCB LAYOUT CONSIDERATIONS

Power Supply Pins For these pins, it is recommended that these be filtered by taking a series 18 ohm resistor and then placing two capacitors shunt to ground, thus creating a low pass filter. Although it makes sense to use large capacitor values in theory, the ESR (Equivalent Series Resistance) is greater for larger capacitors. For optimal filtering minimize the sum of the ESR and theoretical impedance of the capacitor. It is therefore recommended to provide two capacitors of very different sizes for the best filtering. 0.1 µF and 100 pF are typical values. The charge pump supply pins in particular are vuvulnerablenerable to power supply noise.

High Frequency Input Pins, FinRF and FinIF The signal path from the VCO to the PLL is the most sensitive and challenging for board layout. It is generally recommended that the VCO output go through a resistive pad and then through a DC blocking capacitor before it gets to these high frequency input pins. If the trace length is sufficiently short (< 1/10th of a wavelength), then the pad may not be necessary, but a series resistor of about 39 ohms is still recommended to isolate the PLL from the VCO. The DC blocking capacitor should be chosen at least to be 100 pF. It may turn out that the frequency in this trace is above the self-resonant frequency of the capacitor, but since the input impedance of the PLL tends to be capacitive, it actually be a benefit to exceed the self-resonant frequency. The pad and the DC blocking capacitor should be placed as close to the PLL as possible

Complimentary High Frequency Pin, FinRF* These inputs may be used to drive the PLL differentially, but it is very common to drive the PLL in a single ended fashion. A shunt capacitor should be placed at the FinRF* pin. The value of this capacitor should be chosen such that the impedance, including the ESR of the capacitor, is as close to an AC short as possible at the operating frequency of the PLL. 100 pF is a typical value.

FASTLOCK AND CYCLE SLIP REDUCTION

The LMX2471 has enhanced features for Fastlock and cycle slip operation. The next several sections discuss the the benefits of using both of these features. There are four possible combinations that are possible, and these are shown in the table below:

Charge Pump Current	Keep Comparison Frequency the Same	Decrease Comparison Frequency (CSR) (RF Side Only)
Increase Charge Pump Current	Classical Fastlock Allows the loop bandwidth to be increased. This has a frequency glitch caused by switching the charge pump currents, but there is no frequency glitch caused by switching from fractional to integer mode	CSR/Fastlock Combination Engaging the CSR does decrease the loop bandwidth during frequency acquisition, but may be necessary to reduce cycle slipping. By also increasing the charge pump current, this can compensate for the reduce loop bandwidth due to the CSR
Keep Charge Pump Current the Same	Operation with No Fastlock This mode represents using no Fastlock	CSR Only This mode is not generally recommended, but may reduce cycle slipping in some applications. Although the theoretical lock time is decreased, due to the decreased loop bandwidth during Fastlock, cycle slips can be reduced or eliminated.
Decrease Charge Pump Current	It never makes sense to use a lower charge pump current during Fastlock than in the steady state.	

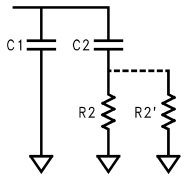
Note that if the charge pump current and cycle slip reduction circuitry are engaged in the same proportion, then it is not necessary to switch in a Fastlock resistor and the loop filter will be optimized for both normal mode and Fastlock mode. For third and fourth order filters which have problems with cycle slipping, this may prove to be the optimal choice of settings.

Determining the Loop Gain Multiplier, K

The loop bandwidth multiplier, K, is needed in order to determine the theoretical impact of fastlock/CSR on the loop bandwidth and also which resistor should be switched in parallel with the loop filter resistor R2. $K = K\_K \cdot K\_Fcomp$ where K is the loop gain multiplier K_K is the ratio of the Fastlock charge pump current to the steady state charge pump current. Note that this should always be greater than or equal to one. K_Fcomp is the ratio of the Fastlock comparison frequency to the steady state comparison frequency. If this ratio is less than one, this implies that the CSR is being used.

Determining the Theoretical Lock Time Improvement and Fastlock Resistor, R2'

When using fastlock, it is necessary to switch in a resistor R2', in parallel with R2 in order to keep the loop filter optimized and maintain the same phase margin. After the PLL has achieved a frequency that is sufficiently close to the desired frequency, the resistor R2' is disengaged and the charge pump current is and comparison frequency are returned to normal. Of special concern is the glitch that is caused when the resistor R2' is disengaged. This glitch can take up a significant portion of the lock time. The LMX2471 has enhanced switching circuitry to minimize this glitch and therefore improve the lock time.



The change in loop bandwidth is dependent upon the loop gain multiplier, K, as determined in section 4. The theoretical improvement in lock time is given below, but the actual improvement will be less than this due to the glitch that is caused by disengaging Fastlock. The theoretical improvement is given to show an upper bound on what improvement is possible with Fastlock. In the case that K < 1, this implies the CSR is being engaged and that the theoretical lock time will be degraded. However, since this mode reduces or eliminates cycle slipping, the actual lock time may be better in cases where the loop bandwidth is small relative to the comparison frequency. Realize that the theoretical lock time multiplier does not account for the fastlock/CSR disengagement glitch, which is most severe for larger values of K.

Loop Gain Multiplier, K	Loop Bandwidth Multiplier	R2' Value	Lock Time Multiplier
1:8*	0.35	open	× 2.828
1:4*	0.50	open	× 2.000
1:2*	0.71	open	× 1.414
4:1	2.00	R2/1.00	× 0.500
8:1	2.83	R2/1.83	× 0.354
16:1	4.00	R2/3.00	× 0.250
32:1	5.66	R2/4.65	× 0.177

* These modes of operation are generally not recommended

Using Fastlock and Cycle Slip Reduction (CSR) to Avoid Cycle Slipping

In the case that the comparison frequency is very large (i.e. 100 X) of the loop bandwidth, cycle slipping may occur when an instantaneous phase error is presented to the phase detector. This can be reduced by increasing the loop bandwidth during frequency acquisition, decreasing the comparison frequency during frequency acquisition, or some combination of the these. If increasing the loop bandwidth during frequency acquisition is not sufficient to reduce cycle slipping, the LMX2471 also has a routine to decrease the comparison frequency.

RF PLL Fastlock Reference Table and Example

The table below shows most of the trade-offs involved in choosing a steady-state charge pump current (RF_CPG), the Fastlock charge pump current (RF_CPF), and the Cycle Slip Reduction Factor (CSR).

Parameter	Advantages to Choosing Smaller	Advantages to Choosing Larger
RF_CPG	1. Allows capacitors in loop filter to be smaller values making it easier to find physically smaller components and components with better dielectric properties.	Phase noise, especially within the loop bandwidth of the system will be slightly worse for lower charge pump currents.
	2. Allows a larger loop bandwidth multiplier for fastlock, or a higher cycle slip reduction factor.	
RF_CPF	The only reason not to always choose this to 1600 µA is to make it such that no resistor is required for fastlock. For 3rd and 4th order filters, it is not possible to keep the filter perfectly optimized by simply switching in a resistor for fastlock.	This allows the maximum possible benefit for fastlock.
CSR	Do not choose this any larger than necessary to eliminate cycle slipping. Keeping this small allows a larger loop bandwidth multiplier for fastlock.	This will eliminate cycle slips better.

The above table shows various combinations for using RF_CPG, RF_CPF, and CSR. Although this table does not show all possible combinations, it does show all the modes that give the best possible performance. To use this table, choose a CSR factor on the horizontal axis, then a fastlock loop bandwidth multiplier on the vertical axis, and the table will show all possible combinations of steady state current, Fastlock current, and what resistor value (R2') to use during Fastlock. In order to better illustrate the cycle slipping and Fastlock circuitry, consider the following example:

Crystal Reference	10 MHz
Comparison Frequency	10 MHz × 2 = 20 MHz (OSC2X = 1)
Output Frequency	1930 – 1990 MHz
PLL Loop Bandwidth	10 KHz
Loop Filter Order	4th (i.e. 7 components)

The comparison frequency is 20 MHz and the loop bandwidth is 10 KHz. 20 MHz is a good comparison freqeuncy to use because it yields the best phase noise performance. This ratio of the comparison frequency to the loop bandwidth is 2000, so cycle slipping will occur and degrade the lock time, unless something is done to prevent it. Because the filter is fourth order, it would be difficult to keep the loop filter optimized if the loop gain multiplier, K was not one. For this reason, choosing a loop gain multiplier of one makes sense. One solution is to set the steady state current to be 100 µA, and the fastlock current to be 1600 µA. The CSR factor could be set to 1/16 and reduce this ratio to 2000/16 = 125. However, using 100 µA charge pump current has phase noise that is significantly worse than the higher charge pump current modes. A better solution would be to use 200 µA current and 1600 µA X2 (using PDCP = X2 Fastlock), since the 200 µA mode will have better phase noise. Depending on how important phase noise is, it could make sense to use a higher steady state current. Using 800 µA steady state current provides much better phase noise than 200 uA (about 5 dB), but then the cycle slip reduction factor would need to be reduced to 4. In general, it is good practice to use the PDCP = X2 fastlock mode whenever cycle slip reduction is used, so that the best phase noise can be achieved. If the ¼ CSR factor is used, then the ratio of comparison frequency to loop bandwidth in fastlock is reduced to 250. There may be some cycle slipping, but the phase noise benefit of using the higher charge pump current may be worth it. If phase noise is even more important, it might even make sense to have a steady state current of 1600 µA and use a CSR factor of ½ and the PDCP mode of X2 Fastlock. Another consideration is that the comparison frequency could be lowered in the steady state mode to reduce cycle slipping. This sacrifices phase noise for lock time. In general, using Fastlock and CSR is not the same for every application. There is a trade-off of lock time vs. phase noise. It might be tempting to try to achieve the best Fastlock benefit by using a K value of 32. Even if the loop filter could be kept well optimized in Fastlock, this hypothetical design would probably switch very fast when the Fastlock was engaged, but then when Fastlock is disengaged, a large frequency glitch would appear, and the majority of the lock time would consist of waiting for this glitch to settle out. Although this would definitely improve the lock time, even accounting for the glitch, the same result could probably be obtained by using a lower K value, like 8, and having better phase noise instead.

Capacitor Dielectric Considerations for Lock Time

The LMX2471 has a high fractional modulus and high charge pump gain for the lowest possible phase noise. One consideration is that the reduced N value and higher charge pump may cause the capacitors in the loop filter to become larger in value. For larger capacitor values, it is common to have a trade-off between capacitor dielectric quality and physical size. Using film capacitors or NP0/CG0 capacitors yields the best possible lock times, where as using X7R or Z5R capacitors can increase lock time by 0 – 500%. However, it is a general tendency that designs that use a higher compare frequency tend to be less sensitive to the effects of capacitor dielectrics. Although the use of lesser quality dielectric capacitors may be unavoidable in many circumstances, allowing a larger footprint for the loop filter capacitors, using a lower charge pump current, and reducing the fractional modulus are all ways to reduce capacitor values. Capacitor dielectrics have very little impact on phase noise and spurs.

FRACTIONAL SPUR AND PHASE NOISE CONTROLS FOR THE LMX2471

The LMX2471 has several bits that have a large impact on fractional spurs. These bits also have a lesser effect on phase noise. The control words in question are CPUD[2:0], FM[1:0], and DITH[1:0]. It is difficult to predict which settings will be optimal for a particular application without testing them, but the general recipe for using these bits can be seen.

A good algorithm is to start with a 3rd order fractional modulator (FM=3) and dithering disabled. Then depending on whether phase noise, fractional spurs, or sub-fractional spurs are most important, optimize the settings. Integer spurs and fractional spurs are nothing new, but sub-fractional spurs are something unique to delta-sigma PLLs. These are spurs that occur at a fraction of the frequency of where a fractional spur would appear.

First adjust the delta-sigma modulator order. Often increasing from a 2nd to a 3rd order modulator provides a large benefit in spur levels. Increasing from a 3rd to a 4th order modulator usually provides some benefit, but it is usually on the order of a few dB. The modulator order by far has the greatest impact on the main fractional spurs. If the loop bandwidth is very wide, or the loop filter order is not high enough, higher order modulators will introduce a lot of sub-fractional spurs. The second order modulator usually does not have these sub-fractional spurs. The third order modulator will introduce them at ½ of the frequency where one would expect to see a traditional fractional spur, thus the name "sub-fractional spur". The fourth order modulator will introduce these spurs at ½ and ¼ of where a traditional fractional spur would be. If the benefit of using a higher order modulator seems significant enough, it may make sense to try to compensate for them using the other two test bits, or designing a higher order loop filter. Be aware that the impact of the modulator order on the spurs may not be consistent across tuning voltage. When the charge pump mismatch is not so bad, the lower order modulators may seem to outperform the higher order modulators, but when the worst case fractional spurs are considered over the whole range, often the higher order modulator performs better.

Second, adjust with the CPUD[2:0] bits. Setting this bit to maximum tends to reduce the sub-fractional spurs the most, however, it may degrade phase noise by up to 1 dB.

Third, experiment with the dithering. When dithering is enabled, it may increase phase noise by up to 2 dB. However, enabling dithering may also reduce the sub-fractional spurs. Also, sometimes both the fractional spurs and the sub-fractional spurs can be unpredictable with dithering disabled. This is because the delta-sigma sequence is periodic, but the starting point changes. Dithering takes these problems away. When the fractional numerator is 0, enabling dithering typically hurts spur performance, because it is trying to correct for spur that are not there.

Fourth, consider experimenting with the loop filter order and comparison frequency. In general, higher order loop filters are always better, but they require more components. Often, the best spur performance is at higher comparison frequencies as well. The reason why this is the last step is not because it has the least impact, but because it takes more labor to do this than to change the FM[1:0], CPUD[2:0], and DITH[1:0] bits.

Although general trends do exist, the optimal settings for test bits may depend on the comparison frequency and loop filter. Also the output frequency in important. In particular, the charge pump tuning voltage is relevant. The recommended way to do this is to test the spur levels at the low, middle, and high range of the VCO, and use the worst case over these three frequencies as a metric for performance. Also, it is important to be aware that all the rules stated above have counterexamples and exceptions. However, more often than not, these rules apply.

PROGRAMMING DESCRIPTION

GENERAL PROGRAMMING INFORMATION

The descriptions below describe the 24-bit data registers loaded through the MICROWIRE Interface. These data registers are used to program the R counter, the N counter, and the internal mode control latches. The data format of a typical 24-bit data register is shown below. The control bits CTL [3:0] decode the register address. On the rising edge of LE, data stored in the shift register is loaded into one of the appropriate latches (selected by address bits). Data is shifted in MSB first. Note that it is best to program the N counter last, since doing so initializes the digital lock detector and Fastlock circuitry. Note that initialize means it resets the counters, but it does NOT program values into these registers. Upon a cold power-up, it is necessary to program all the registers. The exception is when 22-bit is not being used. In this case, it is not necessary to program the R7 register.

MSB					**LSB**
DATA [21:0]		CTL [3:0]			
23	4	3	2	1	0

Register Location Truth Table

The control bits CTL [2:0] decode the internal register address. The table below shows how the control bits are mapped to the target control register.

C3	C2	C1	C0	DATA Location
x	x	x	0	R0
0	0	0	1	R1
0	0	1	1	R2
0	1	0	1	R3
0	1	1	1	R4
1	0	0	1	R5
1	0	1	1	R6
1	1	0	1	R7
1	1	1	1	R8

Control Register Content Map

Because the LMX2471 registers are complicated, they are organized into two groups, basic and advanced. The first four registers are basic registers that contain critical information necessary for the PLL to achieve lock. The last 5 registers are for features that optimize spur, phase noise, and lock time performance. The next page shows these registers.

Quick Start Register Map

Although it is highly recommended that the user eventually take advantage of all the modes of the LMX2471, the quick start register map is shown in order for the user to get the part up and running quickly using only those bits critical for basic functionality. The following default conditions for this programming state are a third order delta-sigma modulator in 22-bit mode with no dithering and no Fastlock.

REGISTER	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	DATA[19:0] (Except for the RF_N Register, which is [22:0])																				C3	C2	C1	C0
R0	RF_N[10:0]											RF_FN[11:0]												0
R1	RF_PD	1	RF_R[5:0]						RF_FD[11:0]												0	0	0	1
R2	IF_PD	IF_P	IF_CPG	IF_N[16:0]																	0	0	1	1
R3	0	RF_CPG[3:0]				IF_R[14:0]															0	1	0	1
R4	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1
R5	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	1
R6	0	0	0	0	0	0	0	0	0	0	1	1	0	0	0	1	0	0	0	0	1	0	1	1
R7	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	1
R8	0	0	0	0	1	1	0	0	0	0	0	0	1	0	0	0	1	1	1	0	1	1	1	1

Complete Register Map

The complete register map shows all the functionality of all registers, including the last five.

REGISTER	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	DATA[19:0] (Except for the RF_N Register, which is [22:0])																				C3	C2	C1	C0
R0	RF_N[10:0]											RF_FN[11:0]												0
R1	RF_PD	1	RF_R[5:0]						RF_FD[11:0]												0	0	0	1
R2	IF_PD	IF_P	IF_CPG	IF_N[17:0]																	0	0	1	1
R3	0	RF_CPG[3:0]				IF_R[14:0]															0	1	0	1
R4	CSR[1:0]		RF_CPF[3:0]				RF_TOC[13:0]														0	1	1	1
R5	0	0	0	1	0	0	0	0	IF_TOC[11:0]												1	0	0	1
R6	0	0	0	0	0	RF_CPT	RF_CPP	IF_CPT	IF_CPP	FDM	FM[1:0]		ATPU[1:0]		OSC 2X	OSC	MUX[3:0]				1	0	1	1
R7	RF_FD2[9:0]										RF_FN2[9:0]										1	1	0	1

R8	0	0	0	0	DITH[1:0]		0	0	0	0	0	0	PDCP[1:0]		0	0	CPUD[2:0]		0	1	1	1	1

R0 REGISTER

Note that this register has only one control bit. The reason for this is that it enables the N counter value to be changed with a single write statement to the PLL.

REGISTER	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	DATA[19:0] (Except for the RF_N Register, which is [22:0])																				C3	C2	C1	C0
R0	RF_N[10:0]											FN[11:0]												0

RF_FN[11:0] -- Fractional Numerator for RF PLL

Refer to section 2.8.1 for a more detailed description of this control word.

RF_N[10:0] -- RF N Counter Value

The RF N counter contains a 16/17/20/21 prescaler. Because there is only one selection of prescaler, the value that is programmed is simply the N counter value converted into binary form. However, because this counter does have a prescaler, there are limitations on the divider values.

RF_N	RF_N[10:0]										
	RF_C							RF_B		RF_A	
≤64	N values less than or equal to 64 are prohibited.										
65-66	Possible only with a second order delta-sigma engine										
67-70	Possible with a second or third order delta-sigma engine.										
71	0	0	0	0	1	0	0	0	1	1	1
72	0	0	0	0	1	0	0	1	0	0	0
...	.	.	.	.	.	.	.	.	.	.	.
2039	1	1	1	1	1	1	1	0	1	1	1
2040-2043	Possible with a second or third order delta-sigma engine.										
2044-2045	Possible only with a second order delta-sigma engine.										
>2045	N values above 2045 are prohibited.										

R1 REGISTER

REGISTER	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	DATA[19:0] (Except for the RF_N Register, which is [22:0])																				C3	C2	C1	C0
R1	RF_PD	1	RF_R[5:0]						RF_FD[11:0]												0	0	0	1

RF_FD[11:0] -- RF PLL Fractional Denominator

The function of these bits are described in section 2.8.2.

RF_R [5:0] -- RF R Divider Value

The RF R Counter value is determined by this control word. Note that this counter does allow values down to one.

R Value	RF_R[5:0]					
1	0	0	0	0	0	1
...	.	.	.	.	.	.
63	1	1	1	1	1	1

RF_PD -- RF Power Down Control Bit

When this bit is set to 0, the RF PLL operates normally. When it is set to one, the RF PLL is powered down and the RF Charge pump is set to a TRI-STATE mode. Because the EN pin and ATPU[1:0] word also controls power down functions, there may be some conflicts. The order of precedence is as follows. First, if the EN pin is LOW, then the PLL will be powered down. Provided this is not the case, the PLL will be powered up if the ATPU[1:0] word says to do so, regardless of the state of the RF_PD bit. After the EN pin and the ATPU[1:0] word are considered, then the RF_PD bit then takes control of the power down function for the RF PLL.

R2 REGISTER

REGISTER	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	DATA[19:0] (Except for the RF_N Register, which is [22:0])																				C3	C2	C1	C0
R2	IF_PD	IF_P	IF_CPG	IF_N[17:0]																	0	0	1	1

IF_N[16:0] -- IF N Divider Value

The IF N divider is a classical dual modulus prescaler with a selectable 8/9 or 16/17 modulus. The IF_N value is determined by the IF_A , IF_B, and IF_P values. Note that the IF_P word can assume a value of 8 or 16. The RF_A and RF_B counter values can be determined in accordance with the following equations.

B = N div P

A = N mod P

B≥A is required in order to have a legal N divider ratio

Here the div operator is defined as the division of two numbers with the remainder disregarded and the mod operator is defined as the remainder as a result of this division. For the purposes of programming, it turns out that the register value is just the binary representation of the N value, with the exception that the 4th LSB is not used and must be programmed to 0 when the 8/9 prescaler is used.

IF_N Programming with the 8/9 Prescaler

N Value	IF_N[16:0]																
	IF_B													IF_A			
<24	N Values Below 24 are prohibited since IF_B≥3 is required.																
24-55	Legal divide ratios in this range are: 24-27, 32-36, 40-45, 48-54																
56	0	0	0	0	0	0	0	0	0	0	1	1	1	0	0	0	0
...	.	.	.	.	.	.	.	.	.	.	.	.	.	0	.	.	.
65535	1	1	1	1	1	1	1	1	1	1	1	1	1	0	1	1	1

RF_N Programming with 16/17 Prescaler

N Value	IF_N[16:0]																
	IF_B													IF_A			
≤47	N values less than or equal to 47 are prohibited because IF_B≥3 is required.																
48-239	Legal divide ratios in this range are: 48-51, 64-68, 80-85, 96-102																
240	0	0	0	0	0	0	0	0	0	0	1	1	1	0	0	0	0
...	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.
131071		1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

IF_CPG -- IF Charge Pump Gain

This bit determines the magnitude of the IF charge pump current

IF_CPG	IF Charge Pump Current (mA)
0	Low (1 mA)
1	High (4 mA)

IF_P -- IF Prescaler Value

This bit selects which prescaler will be used for the IF N counter.

IF_P	IF Prescaler Value
0	8 (8/9 Prescaler)
1	16 (16/17 Prescaler)

IF_PD -- IF Power Down Bit

When this bit is set to 0, the IF PLL operates normally. When it is set to 1, the IF PLL powers down and the output of the IF PLL charge pump is set to a TRI-STATE mode. If the IF_CPT bit is set to 0, then the power down state is synchronous and will not occur until the charge pump is off. If the IF_CPT bit is set to 1, then the power down will occur immediately regardless of the state of the IF PLL charge pump.

R3 REGISTER

REGISTER	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	DATA[19:0] (Except for the RF_N Register, which is [22:0])																				C3	C2	C1	C0
R3	0	RF_CPG[3:0]				IF_R[14:0]															0	1	0	1

IF_R[14:0] -- IF R Divider Value

For the IF R divider, the R value is determined by the IF_R[14:0] bits in the R3 register. The minimum value for IF_R is 3.

R Value	IF_R[14:0]														
3	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1
...	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.
32767	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

RF_CPG -- RF PLL Charge Pump Gain

This is used to control the magnitude of the RF PLL charge pump in steady state operation

RF_CPG[3:0]	RF Charge Pump Current (µA)
0	100
1	200
2	300
3	400
4	500
5	600
6	700
7	800
8	900
9	1000
10	1100
11	1200

12	1300
13	1400
14	1500
15	1600

R4 REGISTER

This register controls the conditions for the RF PLL in Fastlock.

REGISTER	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	DATA[19:0] (Except for the RF_N Register, which is [22:0])																				C3	C2	C1	C0
R4	CSR[1:0]		RF_CPF[3:0]				RF_TOC[13:0]														0	1	1	1

RF_TOC -- RF Time Out Counter and Control for FLoutRF Pin

The RF_TOC[13:0] word controls the operation of the RF Fastlock circuitry as well as the function of the FLoutRF output pin. When this word is set to a value between 0 and 3, the RF Fastlock circuitry is disabled and the FLoutRF pin operates as a general purpose CMOS TRI-STATE I/O. When RF_TOC is set to a value between 4 and 16383, the RF Fastlock mode is enabled and the FLoutRF pin is utilized as the RF Fastlock output pin. The value programmed into the RF_TOC[13:0] word represents four times the number of phase detector comparison cycles the RF synthesizer will spend in the Fastlock state.

RF_TOC[13:0]	Fastlock Mode	Fastlock Period [CP events]	FLoutRF Pin Functionality
0	Disabled	N/A	High Impedance
1	Manual	N/A	Logic “0” State. Forces all fastlock conditions
2	Disabled	N/A	Logic “0” State
3	Disabled	N/A	Logic “1” State
4	Enabled	4X2 = 8	Fastlock
5	Enabled	5X2 = 10	Fastlock
…	Enabled	…	Fastlock
16383	Enabled	16383X2=32766	Fastlock

RF_CPF -- RF PLL Fastlock Charge Pump Current

Specify the charge pump current for the Fastlock operation mode for the RF PLL. Note that the Fastlock charge pump current, steady state current, and CSR control are all interrelated. Refer to section 4.0 for more details.

RF_CPF [3:0]	Fastlock Charge Pump Current (µA)
0000	100
0001	200
0010	300
0011	400
0100	500
0101	600
0110	700
0111	800
1000	900
1001	1000
1010	1100
1011	1200
1100	1300
1101	1400
1110	1500

1111	1600

RF_CSR[1:0] -- RF Cycle Slip Reduction

CSR controls the operation of the Cycle Slip Reduction Circuit. This circuit can be used to reduce the occurrence of phase detector cycle slips. Note that the Fastlock charge pump current, steady state current, and CSR control are all interrelated. The table below gives some rough guidelines. In the table below, f_{COMP} is the comparison frequency, and BW is the loop bandwidth of the PLL system. The rough guideline gives an idea of when it makes sense to use this cycle slip reduction based on the steady-state conditions of the PLL system.

CSR[1:0]	CSR State	Sample Rate Reduction Factor	Rough Guideline
0	Disabled	1	$f_{COMP} < 100 \times BW$
1	Enabled	1/2	$100 \times BW < f_{COMP} < 200 \times BW$
2	Enabled	1/4	$200 \times BW < f_{COMP} < 400 \times BW$
3	Enabled	1/16	$f_{COMP} > 400 \times BW$

R5 REGISTER

REGISTER	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	DATA[19:0] (Except for the RF_N Register, which is [22:0])																				C3	C2	C1	C0
R5	0	0	0	0	0	0	0	0	IF_TOC[11:0]												1	0	0	1

IF_TOC[11:0] IF Timeout Counter for Fastlock

The IF_TOC word controls the operation of the IF Fastlock circuitry as well as the function of the FLoutIF output pin. When IF_TOC is set to a value between 0 and 3, the IF Fastlock circuitry is disabled and the FLoutIF pin operates as a general purpose CMOS TRI-STATE output. When IF_TOC is set to a value between 4 and 4095, the IF Fastlock mode is enabled and FLoutIF is utilized as the IF Fastlock output pin. The value programmed into IF_TOC represents the number of phase comparison cycles that the IF synthesizer will spend in the Fastlock state.

IF_TOC[11:0]	Fastlock Mode	Fastlock Period [Charge Pump Cycles]	FLoutIF Pin Functionality
0	Disabled	N/A	High Impedance
1	Manual	N/A	Logic “0” State Forces IF charge pump current to 4 mA
2	Disabled	N/A	Logic “0” State
3	Disabled	N/A	Logic “1” State
4	Enabled	5	Fastlock
…	Enabled	…	Fastlock
4095	Enabled	4095	Fastlock

R6 REGISTER

REGISTER	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	DATA[19:0] (Except for the RF_N Register, which is [22:0])																				C3	C2	C1	C0
R6	0	0	0	0	0	RF_CPT	RF_CPP	IF_CPT	IF_CPP	FDM	FM[1:0]		ATPU [1:0]		OSC 2X	OSC	MUX [3:0]				1	0	1	1

MUX[3:0] Frequency Out & Lock Detect MUX

These bits determine the output state of the Ftest/LD pin.

MUX[3:0]				Output Type	Output Description
0	0	0	0	High Impedance	Disabled

0	0	0	1	Push-Pull	General purpose output, Logical “High” State
0	0	1	0	Push-Pull	General purpose output, Logical “Low” State
0	0	1	1	Push-Pull	RF & IF Digital Lock Detect
0	1	0	0	Push-Pull	RF Digital Lock Detect
0	1	0	1	Push-Pull	IF Digital Lock Detect
0	1	1	0	Open Drain	RF & IF Analog Lock Detect
0	1	1	1	Open Drain	RF Analog Lock Detect
1	0	0	0	Open Drain	IF Analog Lock Detect
1	0	0	1	Push-Pull	RF & IF Analog Lock Detect
1	0	1	0	Push-Pull	RF Analog Lock Detect
1	0	1	1	Push-Pull	IF Analog Lock Detect
1	1	0	0	Push-Pull	IF R Divider divided by 2
1	1	0	1	Push-Pull	IF N Divider divided by 2
1	1	1	0	Push-Pull	RF R Divider divided by 2
1	1	1	1	Push-Pull	RF N Divider divided by 2

OSC -- Differential Oscillator Mode Enable

This bit selects between single-ended and differential mode for the OSCin and OSCout* pins. When this bit is set to 0, the RF R and IF R counters are driven in a single-ended fashion through the OSCin pin. Note that the OSCin and OSCout* pin can not be used to drive a crystal. When this bit is set to 1, the OSCin and OSCout* pins are used to drive these R counters differentially. In some cases, spur performance may be better when this is set to differential mode, even if the R counters are being driven in a single-ended fashion. Current consumption in differential mode is slightly higher than when in single-ended mode.

OSC2X -- Oscillator Doubler Enable

When this bit is set to 0, the oscillator doubler is disabled TCXO frequency presented to the IF R counter is unaffected. Phase noise added by the doulber is negligible.

ATPU -- PLL Automatic Power Up

This word enables the PLLs to be automatically powered up when their respective registers are written to. Note that since the IF Powerdown bit is in the IF register, there is no need to have an ATPU function activated by the R2 word.

ATPU	RF PLL	IF PLL
0	No auto power up	No auto power up
1	Powers up when R0 is written to	No auto power up
2	Powers up when R0 is written to	Powers up when R0 is written to
3	Reserved	

FM[1:0] -- Fractional Mode

Determines the order of the delta-sigma modulator. Higher order delta-sigma modulators reduce the spur levels closer to the carrier by pushing this noise to higher frequency offsets from the carrier. In general, the order of the loop filter should be at least one greater than the order of the delta-sigma modulator in order to allow for sufficient roll-off.

FM	Function
0	Fractional PLL mode with a 4th order delta-sigma modulator
1	Disable the delta-sigma modulator. Recommended for test use only.
2	Fractional PLL mode with a 2nd order delta-sigma modulator
3	Fractional PLL mode with a 3rd order delta-sigma modulator

FDM -- Fractional Denominator Mode

When this bit is set to 0, the part operates with a 12- bit fractional denominator. For most applications, 12-bit mode should be adequate, but for those applications requiring ultra fine tuning resolution, there is 22-bit mode. Note that the PLL may consume slightly more current when it is in 22-bit mode.

FDM	Bits for Fractional Denominator/Numerator	Maximum Size of Fractional Denominator/Numerator
0	12-bit	4095
1	22-bit	4194303

IF_CPP -- IF PLL Charge Pump Polarity

When this bit is set to 1, the phase detector polarity for the IF PLL charge pump is positive. Otherwise set this bit to 0 for a negative phase detector polarity

IF_CPT -- IF PLL Charge Pump TRI-STATE Mode

This bit enables the user to put the charge pump in a TRI-STATE (high impedance) condition. Note that if there is a conflict, the ATPU bit overrides this bit.

RF_CPT	Charge Pump State
0	ACTIVE
1	TRI-STATE

RF_CPP -- RF PLL Charge Pump Polarity

For a positive phase detector polarity, which is normally the case, set this bit to 1. Otherwise set this bit to 0 for a negative phase detector polarity.

RF_CPT -- RF PLL Charge Pump TRI-STATE Mode

This bit enables the user to put the charge pump in a TRI-STATE (high impedance) condition. Note that if there is a conflict, the ATPU bit overrides this bit.

RF_CPT	Charge Pump State
0	Active
1	TRI-STATE

R7 REGISTER

REG ISTER	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	DATA[19:0]																				C3	C2	C1	C0
R7	RF_FD2[9:0]										RF_FN2[9:0]										1	1	0	1

Fractional Numerator Determination { RF_FN2[9:0], RF_FN[11:0], FDM }

In the case that the FDM bit is 0, then the part operates in 12-bit fractional mode, and the RF_FN2 bits become don't care bits. When the FDM is set to 1, the part operates in 22-bit mode and the fractional numerator is expanded from 12 to 22-bits.

Fractional Numerator	RF_FN2[9:0] (These bits only apply in 22- bit mode)										RF_FN[11:0]											
0	In 12- bit mode, these are don't care. In 22- bit mode, for N <4096, these bits should be all set to 0.										0	0	0	0	0	0	0	0	0	0	0	0
1											0	0	0	0	0	0	0	0	0	0	0	1
...											.	.	.	.	.	.	.	.	.	.	.	.
4095											1	1	1	1	1	1	1	1	1	1	1	1
4096	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0
...	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.
4194303	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Fractional Denominator Determination { RF_FD2[9:0], RF_FD[11:0], FDM }

In the case that the FDM bit is 0, then the part is operates in the 12-bit fractional mode, and the RF_FD2 bits become don't care bits. When the FDM is set to 1, the part operates in 22-bit mode and the fractional denominator is expanded from 12 to 22-bits.

Fractional Denominator	RF_FD2[9:0] (These bits only apply in 22- bit mode)										RF_FD[11:0]											
0	In 12- bit mode, these are don't care. In 22- bit mode, for N <4096, these bits should be all set to 0.										0	0	0	0	0	0	0	0	0	0	0	0
1											0	0	0	0	0	0	0	0	0	0	0	1
...											.	.	.	.	.	.	.	.	.	.	.	.
4095											1	1	1	1	1	1	1	1	1	1	1	1
4096	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0
...	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.
4194303	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

R8 REGISTER

	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	DATA[19:0]																				C3	C2	C1	C0
R8	0	0	0	0	DITH [1:0]		0	0	0	0	0	0	PDCP [1:0]		0	0	CPUD [2:0]			0	1	1	1	1

The R8 Register controls some additional bits that may be useful in optimizing phase noise, lock time, and spurs.

CPUD[2:0] -- Charge Pump User Definition

This bit allows the user to choose from several different modes in the charge pump. The charge pump current is unaffected, but the fractional spurs and phase noise are impacted by a few dB. In some designs, particularly if the loop bandwidth is wide and a 4th order delta-sigma engine is used, small spurs may appear at a fraction of where the first fractional spur should appear. In other designs, these sub-fractional spurs are not present. The user needs to use this adjustment to make these sub-fractional spurs go away, while still getting the best phase noise possible.

CPUD	Mode Name	Phase Noise	Sub-Fractional Spurs
0	Reserved	N/A	N/A
1	Reserved	N/A	N/A
2	Minimum	Best	Worst
3	Maximum	Worst	Best

4	Reserved	N/A	N/A
5	Reserved	N/A	N/A
6	Reserved	N/A	N/A
7	Nominal	Medium	Medium

PDCP[1:0] -- Power Drive for Charge Pump

If this bit is enabled, the Fastlock current can be doubled during Fastlock. The charge pump current in steady state is unaffected. States 0 and 1 should never be used.

PDCP	Fastlock Charge Pump Current
0	Reserved
1	Reserved
2	Double Fastlock Current
3	Disabled

DITH[1:0] -- Dithering Control

Dithering is a technique used to spread out the spur energy. Enabling dithering can reduce the main fractional spurs, but can also give rise to a family of smaller spurs. Whether dithering helps or hurts is application specific. Enabling the dithering may also increase the phase noise. In most cases where the fractional numerator is zero, dithering usually degrades performance.

Dithering tends to be most beneficial in applications where there is insufficient filtering of the spurs. This often occurs when the loop bandwidth is very wide or a higher order delta-sigma modulator is used. Dithering tends not to impact the main fractional spurs much, but has a much larger inpact on the sub-fractional spurs. If it is decided that dithering will be used, best results will be obtained when the fractional denominator is at least 1000.

DITH	Dithering Mode Used
0	Dithering Enabled
1	Reserved
2	Reserved
3	Dithering Disabled

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